CLAIMS

What is claimed is:

1. An apparatus comprising:

an amplifier;

a gain circuit coupled to an output of the amplifier, the gain circuit to provide at least two gain values in response to the output of the amplifier; and

a control circuit to provide one of the at least two gain values as an output.

2. The apparatus as claimed in claim 1, wherein the gain circuit includes at least two equalization circuits each providing a respective one of the at least two gain values.

3. The apparatus as claimed in claim 2, wherein the at least two equalization circuits are coupled in series to the output of the amplifier.

4. The apparatus as claimed in claim 2, wherein each of the at least two equalization circuits include an RC filter.

5. The apparatus as claimed in claim 4, wherein a resistance R and a capacitance C of the RC filter are implemented using on-chip components.

6. The apparatus as claimed in claim 4, wherein a resistance R of the RC filter is implemented using passive components.

7. The apparatus as claimed in claim 4, wherein a resistance R of the RC filter is implemented using active components.

8. The apparatus as claimed in claim 4, wherein all resistors in the apparatus are formed of a same technology.

9. The apparatus as claimed in claim 8, wherein the same technology is a poly resistance technology

10. The apparatus as claimed in claim 4, wherein R and C values of the RC filter are fixed during a circuit design phase.

11. The apparatus as claimed in claim 1, wherein the amplifier is a CMOS amplifier and the gain circuit is a CMOS gain circuit.

12. The apparatus as claimed in claim 11, wherein the gain circuit includes at least two equalization circuits each providing a respective one of the at least two gain values.

13. The apparatus as claimed in claim 12, wherein the at least two equalization circuits are coupled in series to the output of the amplifier.

14. The apparatus as claimed in claim 13, wherein each of the at least two equalization circuits include an RC filter.

15. The apparatus as claimed in claim 1, wherein the control circuit includes a DC feedback circuit and the output provided by the control circuit is selected in response to the DC feedback circuit.

16. The apparatus as claimed in claim 15, wherein the DC feedback circuit uses DC balance to help select the output.

17. A system comprising:

a transmitter;

a receiver; and

an interconnect coupled to the transmitter and the receiver;

wherein the receiver includes an equalization circuit comprising:

an amplifier;

a gain circuit coupled to an output of the amplifier, the gain circuit to provide at least two gain values in response to the output of the amplifier; and

a control circuit to provide one of the at least two gain values as an output..

18. The system as claimed in claim 17, wherein the gain circuit includes at least two equalization circuits each providing a respective one of the at least two gain values.

19. The system as claimed in claim 18, wherein the at least two equalization circuits are coupled in series to the output of the amplifier.

20. The system as claimed in claim 18, wherein each of the at least two equalization circuits include an RC filter.

21. The system as claimed in claim 17, wherein the amplifier is a CMOS amplifier and the gain circuit is a CMOS gain circuit.

22. The system as claimed in claim 21, wherein the gain circuit includes at least two equalization circuits each providing a respective one of the at least two gain values.

23. The system as claimed in claim 22, wherein the at least two equalization circuits are coupled in series to the output of the amplifier.

24. The system as claimed in claim 23, wherein each of the at least two equalization circuits include an RC filter.

25. The system as claimed in claim 17, wherein the control circuit includes a DC feedback circuit and the output provided by the control circuit is selected in response to the DC feedback circuit.

26. The system as claimed in claim 25, wherein the DC feedback circuit uses DC balance to help select the output.

27. A method comprising:

providing at least two discrete gain signals; and

adaptively selecting one of the gain signals as an output signal.

28. The method as claimed in claim 27, wherein the at least two discrete gain signals are providing using equalization.

29. The method as claimed in claim 28, wherein the equalization is performed in a cascaded fashion.

30. The method as claimed in claim 29, wherein the cascaded equalization includes an RC filter technique.

31. The method as claimed in claim 27, wherein the selecting is performed based on DC feedback.

32. The method as claimed in claim 31, wherein the DC feedback uses DC balance to help select the output.